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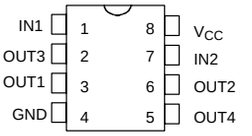
DALLAS SEMICONDUCTOR

DS1012
2-in-1 Sub-Miniature Silicon Delay Line with Logic

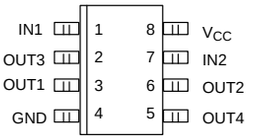
FEATURES

- All-silicon time delay
- 53 µW max. CMOS quiescent mode
- Surface mount 8-pin mini-SOIC and standard 8-pin DIP
- 2 independent buffered delays per input
- Option of complemented output(s)
- Option of timed AND, NAND, OR, NOR, XOR, XNOR, HALF-XOR and HALF-XNOR logic outputs
- Delay tolerance: ±1.5 ns (delays: 3-10 ns), ±2.0 ns (delays: 11-40 ns)
- Vapor phase, IR and wave solderability
- Economical
- TTL/CMOS-compatible
- Quick turn prototypes
- Custom delays and logic options available

PIN ASSIGNMENT



DS1012M 8-PIN DIP (300 MIL)
See Mech. Drawings Section



DS1012Z 8-PIN SOIC (150 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

IN1, IN2	–	Inputs
OUT1, OUT2	–	Outputs (delays)
OUT3, OUT4	–	Outputs (delays, logic)
GND	–	Ground
V_{CC}	–	+5 Volts

DESCRIPTION

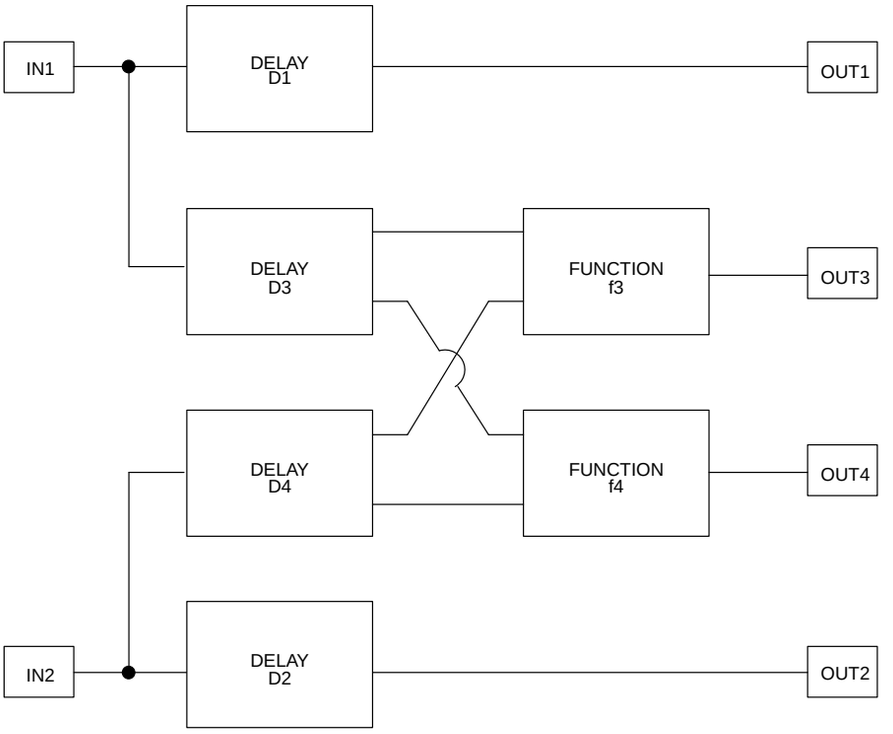
In its most simple configuration, the DS1012 2-in-1 Sub-Miniature Silicon Delay Line Chip provides two inputs, each of which in turn provides independent delays to a pair of outputs. The DS1012-1 and DS1012-3 are examples of catalog parts having this basic configuration. Any of the four outputs can be inverted at the time of manufacture.

For applications requiring two-input timed logic functions, at the time of manufacture the simple delay on OUT4 can be replaced by one of the following: OR, NOR, XOR, or XNOR. Similarly, a timed AND, NAND, HALF-XOR (D3 AND $\overline{D4}$), or NOT HALF-XOR ($\overline{D3}$ OR D4) can be substituted for the simple delay on OUT3. DS1012-2, DS1012-4, and DS1012-5 are examples of catalog parts configured with logic functions on OUT3 and OUT4. Note that DS1012-2 also utilizes an output inversion on OUT2.

In any configuration, delays D1 (t_{D1}) and D2 (t_{D2}) can be specified within the range of ~3 ns to 10 ns. Delays D3 (t_{D3}) and D4 (t_{D4}) can be specified to have values between ~3 ns and 40 ns. The worst case leading edge delay accuracy at nominal voltage and room temperature is ±2 ns. The DS1012 is offered in two packages: an 8-pin DIP and an 8-pin 150 mil wide mini-SOIC.

Dallas Semiconductor offers the DS1012 in a wide variety of custom delay and logic configurations. For special requests and quick turn delivery, call (972) 371–4348.

LOGIC DIAGRAM Figure 1



Function f3 can be one of the following:

D3	$\overline{D3}$
D3 AND D4	D3 NAND D4
D3 HALF-XOR D4	D3 HALF-XNOR D4

Function f4 can be one of the following:

D4	$\overline{D4}$
D3 OR D4	D3 NOR D4
D3 XOR D4	D3 XNOR D4

NOTE: Any output(s) can be inverted at time of manufacture.
If D1 > 10 ns, D1 = D3.
If D2 > 10 ns, D2 = D4.

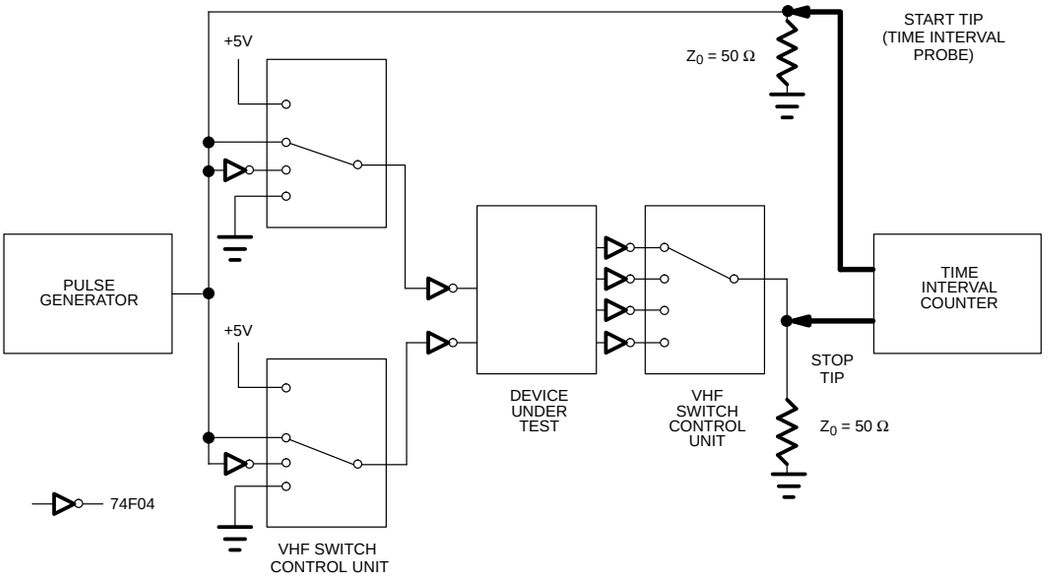
PART NUMBER DELAY AND CONFIGURATION Table 1

CATALOG P/N	t_{D1} (ns)	t_{D2} (ns)	t_{D3} (ns)	t_{D4} (ns)	OUT1	OUT2	OUT3	OUT4
DS1012-1	5	5	10	10	D1	D2	D3	D4
DS1012-2	5	5	10	10	D1	$\overline{D2}$	D3.D4	D3+D4
DS1012-3	3	7	10	40	D1	D2	D3	D4
DS1012-4	5	5	25	25	D1	D2	D3HXD4	D3XD4
DS1012-5	10	10	5	5	D1	D2	D3.D4	D3+D4
DS1012-7	15	4	4	14	D1	$\overline{D2}$	D3	D3XD4
DS1012–9	5	25	5	25	D1	D2	$\overline{D3HXD4}$	D3XD4
DS1012-D16	4	19.6	4	19.6	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D20	4	16.5	4	16.5	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D25	4	14	4	14	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D33	4	11.5	4	11.5	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-D50	4	9	4	9	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-V20	25	50	25	50	D1	D2	$\overline{D3.D4}$	$\overline{D3+D4}$
DS1012-V40	12.5	25	12.5	25	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-V50	10	20	10	20	D1	D2	$\overline{D3.D4}$	D3XD4
DS1012-V60	8.3	8.3	8.3	8.3	D1	D2	$\overline{D3.D4}$	$\overline{D3+D4}$

NOTE: . = AND, + = OR, X = XOR, HX = HALF–XOR

Contact Dallas Semiconductor for information on custom configurations and timing delays.

TEST CIRCUIT Figure 2



TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters on the DS1012. The input waveform is produced by a precision pulse generator under software control connected to the inputs by VHF switch control units. Time delays are measured by a time interval counter (20 ps resolution) connected between the inputs and the outputs. Outputs are connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohms max.
Rise and Fall Time:	3.0 ns max.
Pulse Width:	50 ns
Period:	100 ns

OUTPUT:
Each output is loaded with a 74F04. Delay is measured between the 1.5V level of the rising edge of the input signal and the 1.5V level of the corresponding edge of the output.

NOTE: These conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	TEST	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC}+0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC1}	V_{CC} = MAX; PERIOD = MIN		40.0	70.0	mA	2
Quiescent Current	I_{CC2}	V_{CC} = MAX.			10	µA	5
High Level Output Current	I_{OH}	V_{CC} = MIN V_{OH} = 2.4V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC} = MIN. V_{OL} = 0.5V	8.0			mA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5V ± 5%)

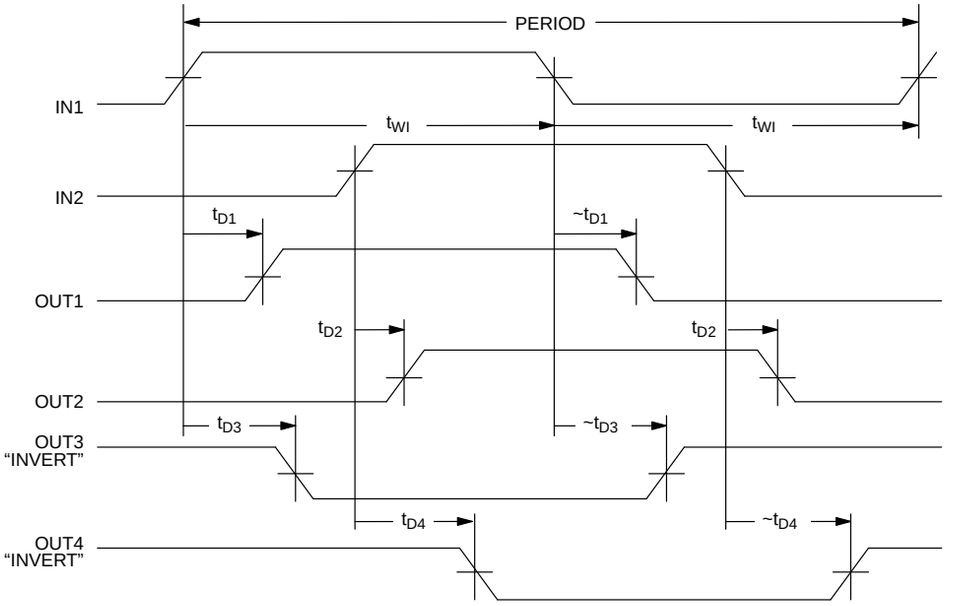
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}				ns	6
Input to Output (leading edge)	t_{D1}, t_{D2}, t_{D3}, t_{D4}				ns	3, 4
Power-up Time	t_{PU}			0	ns	7
	Period	2(t_{WI})			ns	

CAPACITANCE

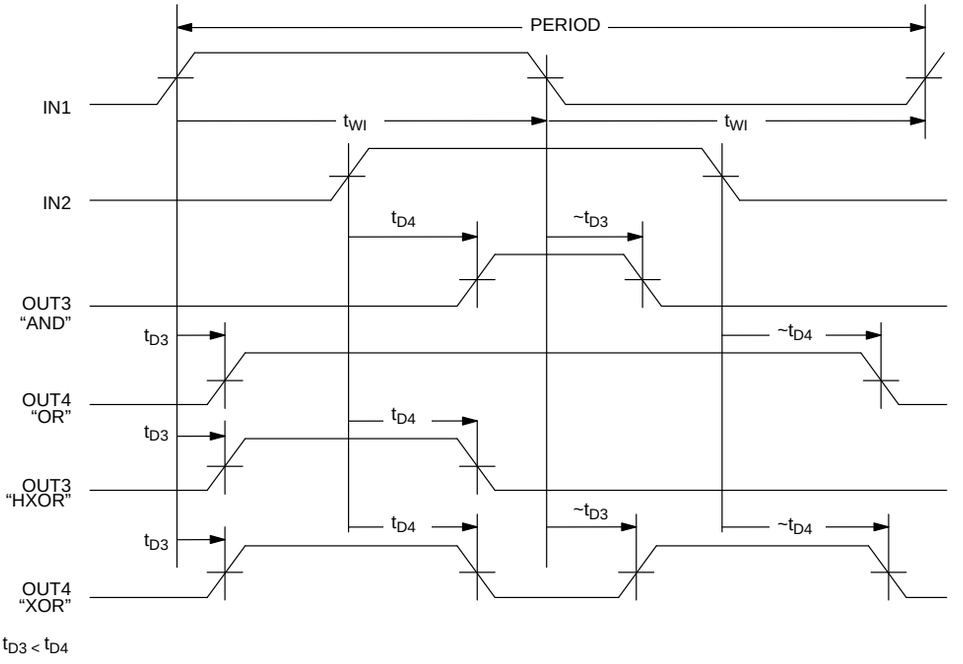
(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

DELAY FUNCTION Figure 3



LOGIC FUNCTIONS Figure 4



NOTES:

1. All voltages are referenced to ground.
2. Measured with outputs open, minimum period. I_{CC1} (max.) for any value of Period can be calculated using the formula:

   I_{CC1} (max.) = 840/Period + I_{CC2}

   where I_{CC1}, I_{CC2} in mA, Period in ns

   Example: If Period = 50 ns then

   I_{CC1} (Max) = 840/50 + 0.01 = 16.81 mA
3. V_{CC} = 5V @ 25°C. Delays referenced to leading (input rising) edges are accurate within ±1.5 ns for values between 3 to 10 ns and ±2 ns for values between 11 to 40 ns. Delays referenced to trailing (input falling) edges will typically equal the corresponding leading edge delay within ±1 ns.
4. See the section entitled “Test Conditions.”
5. For the quiescent mode, both inputs must meet the conditions
   $0.3V > V_I$ or $VI > V_{CC} - 0.3$
6. For specified accuracy, t_{WI} (min) is the longer of $3(t_{D1})$, $3(t_{D2})$, $3(t_{D3})$, or $3(t_{D4})$. Pulse doublers designed for single frequency use will meet specified accuracies at 50% duty cycle; i.e., $2(t_{WI})$ = 1/FREQ = PERIOD. Customs will be adjusted to be accurate at customer input width specifications when t_{WI} is longer than t_{D1}, t_{D2}, t_{D3}, and t_{D4}.
7. On power-up, the DS1012 will supply timing and logic functions with specified accuracy as soon as V_{CC} achieves nominal value.